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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,141	08/29/2005	Giovanni Tricomi	3000-0011	5064

50811 7590 03/02/2009

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EXAMINER	
HUBER, ROBERT T	
ART UNIT	PAPER NUMBER
2892	
MAIL DATE	DELIVERY MODE
03/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,141	TRICOMI ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8 and 13-21* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 4, 2008 has been entered.

Election/Restrictions

2. Newly submitted claims 18 – 21 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: This application contains claims directed to the following patentably distinct species:

a. **Species A**, directed to **claims 16, 17, 2 -8, and 13 – 15** a metallic carrier device.

b. **Species B**, directed to **claims 18 - 21**, a non-conductive carrier device.

The species are independent or distinct because claims to the different species recite the mutually exclusive characteristics of such species. In particular, the originally presented claim 17 recites a "*metallic carrier device*", which is mutually exclusive from the newly presented *"non-conductive carrier device*" of claim 18 (i.e. the carrier device cannot be both 'metallic' and 'non-conductive' since metals are inherently conductive). In addition, these species are not obvious variants of each other based on the current

record. Currently, no claims appear to be generic, since claim 18 does not incorporate all the limitations of claims 16 or 17 (see MPEP 806.04(d)).

There is an examination and search burden for these patentably distinct species due to their mutually exclusive characteristics. The species require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search queries); and/or the prior art applicable to one species would not likely be applicable to another species; and/or the species are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 18 – 21 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

3. The Examiner acknowledges the drawings filed on December 4, 2008. The objection(s) to the drawings cited in the previous office action filed on July 11, 2008 is (are) hereby withdrawn.

Claim Objections

4. The Examiner acknowledges the amendment(s) to the claims filed on December 4, 2008. The objection(s) to claims 2 – 8 and 13 - 15 cited in the previous office action filed on July 11, 2008 is (are) hereby withdrawn.

Claim Rejections - 35 USC § 112

5. The Examiner acknowledges the amendment(s) to the claims filed on December 4, 2008. The rejections of claims 8 and 15 under 35 U.S.C. 112 cited in the previous office action filed on July 11, 2008 is (are) hereby withdrawn.

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. **Claims 18 – 21** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 18 claims "*a non - conductive carrier device*", which was not originally disclosed in the specification or original claim set. No where in the specification is there indicated that the carrier device is non-conducting. On the contrary, in the originally filed claim 17, and page 2 of the specification the applicant discloses that the carrier device is a "*metallic carrier device*", which is inherently

conductive. The carrier cannot be both conducting or non-conducting. Therefore, the Applicant is adding new matter. Claims 19 – 21 depend on claim 18.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. **Claim 2 – 8 and 13 – 17** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 16 recites "*a carrier device comprising a die paddle onto which the die is attached and a plurality of metallic leads....where the carrier device, the die paddle, and the stamped pedestals form a single piece unitary structure*". It is unclear and ambiguous whether the "*plurality of metallic leads*" are a part of the carrier device, or if they are separate, distinct structures. Figure 3 and page 16 of the specification indicate that the "*plurality of metallic leads*" **8**, **9**, and **10** are separate and distinct structures from the carrier **1**. Therefore, a best-deemed interpretation is made, and "*a plurality of metallic leads*" is interpreted to be separate structures from the "*carrier device*". A similar interpretation is made for the "*metallic carrier device*" and "*plurality of metal leads*" of claim 17. Claims 2 - 8 and 15 depend on claim 16, and claims 13 and 14 depend on claim 17.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 16, 2 – 7, 13, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard et al. (US 5,479,050, prior art of record on IDS dated April 11, 2005) in view of Kwon et al. (US 5,365,409, prior art of record).

a. Regarding claim 16, **Prichard discloses an integrated circuit** (e.g. figure 1), **comprising:**

a semiconductor die (die 11);

a carrier device comprising a die paddle onto which the die is attached (paddle 16, disclosed in col. 1, line 65, which is the portion of leadframe 10 under semiconductor die 11) **and a plurality of leads** (leads 17 and 19) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** (outer portion furthest away from the die),

where a plurality of stamped pedestals (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle** (e.g. as seen in figure 1, the pedestals 12 and 13 exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece) ;

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 15), **and a second bond wire extending to an inner lead portion** (bond wire 22).

Pritchard is silent with respect to explicitly disclosing that the plurality of leads are metallic, the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion, and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156); **and a package that encapsulates the semiconductor die, the die paddle, the first and second**

bond wires and the inner lead portions (e.g. as seen in figure 5, there is a package, denoted by a dashed line, that encapsulates the die, paddle, wires and inner lead portions).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that a package encapsulates the die, die paddle, inner lead portions, and bond wires since it was well known in the art that semiconductor structures are encapsulated in such a manner, as supported by Kwon. One would have been motivated to encapsulate the structure in order to protect the inner device elements from external stresses.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard

such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

b. Regarding claim 2, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein the stamped pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle** (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewall has an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

c. Regarding claim 3, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device** (e.g. as seen in figure 3 of Pritchard) **and each has an area for connection of a single bonding wire** (e.g. as seen in figure 1 of Pritchard, there is an area surrounding the bond wire connection on the pedestals 12 and 13 for connecting a single bond wire 14 or 15).

d. Regarding claim 4, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, wherein a height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times the height of the semiconductor die** (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die, and therefore are within the claimed range).

e. Regarding claim 5, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, as cited above, but is silent with respect to a height of each of the raised pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device. Pritchard and Kwon show that the height of the pedestal may be about 0.5 times the height of the carrier device, but it is not explicitly stated.**

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the pedestals are within the range of 1/10 to 2 times the height of the carrier device, since Pritchard and Kwon suggests through the figure this may be the case, and it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would have been motivated to make the height of the pedestal within the range of the carrier device in order to reduce lead length and stress on the leads.

f. Regarding claims 6 and 7, **Kwon discloses the structural limitations of the integrated circuit, as cited in claim 16. The process by which the raised pedestal is formed is not given patentable weight since the patentability of a product does not depend on the method of production. See MPEP 2113.**

g. Regarding claim 17, **Pritchard discloses an integrated circuit** (e.g. figure 1), **comprising:**

a semiconductor die (die 11);

a carrier device comprising a planar surface onto which the die is attached (paddle 16, disclosed in col. 1, line 65, which is the portion of leadframe 10 under semiconductor die 11) **and a plurality of leads** (leads 17 and 19) **each comprising an inner lead portion** (inner portion towards the die) **that extends to an outer lead portion** outer portion furthest away from the die), **where a plurality of stamped pedestals** (pedestals 12 and 13, disclose in col. 1, lines 65 – 67 to be stamped) **are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface** (e.g. as seen in figure 1, the pedestals 12 and 13 exteriorly surround and are adjacent to the top of the die paddle region under the semiconductor die 11), **where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure** (e.g. as seen in the figure, the carrier device, die paddle, and stamped pedestals are formed from a single piece); **and**

a first bond wire extending from the die to a first of the plurality of stamped pedestals (bond wire 15)**, and a second bond wire extending to an inner lead portion** (bond wire 22).

Pritchard is silent with respect to explicitly stating that the carrier device and the plurality of leads are "metallic", and the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion.

Kwon discloses an integrated circuit structure (e.g. figure 5), **comprising a first bond wire** (bond wire 160) **extending from the die** (die 154) **to a first of the plurality of pedestals** (pedestals 158), **and a second bond wire** (bond wire 162) **extending from the first of the plurality of pedestals to an inner lead portion** (inner lead portion of lead 156).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made. One would have been motivated to form a wire bond between the semiconductor die and the pedestal, and between the pedestal and the inner portion of the lead in order to relieve the wire bond of stress formed by making a direct connection between the semiconductor die and the inner portion of the lead.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to use a metallic material in the carrier device of Pritchard, since Pritchard discloses connecting leads to the carrier device (stamped pedestals) to form an electrical circuit, and it has been held by the courts that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. *In re Leshin*, 125 USPQ 416 (CCPA 1960) and *Sinclair & Carroll Co. v. Interchemical Corp.*, 65 USPQ 297 (1945). One would have been motivated to make the carrier device metallic in order to create a conductive portion of the carrier to complete an electrical circuit, as well as allowing the pedestals to be formed easily by stamping.

Furthermore, although Pritchard does not explicitly disclose forming the surrounding leads from metal, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard such that the surrounding leads were formed from metal since Pritchard discloses connecting the leads to the die via wire bonds to form an electrical circuit, and it has been held that selection of a prior art material on the basis of its suitability for its intended purpose is within the level of ordinary skill. See MPEP 2144.07. One would have been motivated to use metal for the surrounding leads since it is electrically conductive, durable, and inexpensive.

h. Regarding claim 13, **Pritchard in view of Kwon discloses the integrated circuit of claim 17, as cited above, where the stamped pedestals**

make an angle (α) greater than 45 degrees with the plane of the carrier device at all sidewalls (e.g. figures 1 and 3 of Pritchard show the angle of the pedestal sidewalls have an angle of 90 (figure 1) and greater than 45 degrees (figure 3) with respect to the top or bottom plane of the die paddle).

Pritchard and Kwon are silent with respect to explicitly stating the sides have rounded junctions parallel to the plane of the carrier device or being rounded as a whole.

However, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that the sides of the pedestals to have rounded junctions parallel to the plane of the carrier device or are rounded as a whole, since it has been held by the courts that a change in shape or configuration, without any criticality, is nothing more than one of numerous shapes that one of ordinary skill in the art will find obvious to provide based on the suitability for the intended final application. See *In re Dailey*, 149 USPQ 47 (CCPA 1976). It appears that the disclosed device of Kwon would perform equally well shaped as disclosed by the Applicant. One would have been motivated to have rounded pedestals since materials deposited often have rounded edges due to the formation process.

i. Regarding claim 14, **Pritchard in view of Kwon disclose the integrated circuit of claim 17, as cited above, where the height of the stamped pedestals lies in the range between 1/10 of the die height and the die height**

itself (as seen in figure 3 and disclosed in col. 2, lines 15 - 17 of Pritchard, the stamped pedestals have a height the same as the semiconductor die).

13. Claims 8 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Pritchard in view of Kwon, and in further view of Carter, Jr. et al. (US 6,365,976 B1, prior art of record).

a. Regarding claim 8, **Pritchard in view of Kwon disclose the integrated circuit of claim 16, but are silent with respect to a silver or gold finish applied to the stamped pedestals.**

Carter discloses that gold or silver finishes may be applied to raised pedestals in integrated circuits (Col. 5, lines 18 - 22, disclose that the surface of the pedestals have a foil on them which may consist of silver or gold, or the pedestal may be covered with a tin-silver layer).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

b. Regarding claim 15, **Pritchard in view of Kwon disclose an integrated circuit, but are silent with respect to only in the areas of the stamped pedestals, a finish, particularly silver or gold, is provided for bondability.**

Carter discloses that areas of pedestals may be provided with a gold or silver finish (col. 5, lines 20 - 22, discloses that the pedestal ("dimple") may covered with a layer of tin-silver).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device of Pritchard in view of Kwon such that there is a gold or silver finish on the raised pedestals since it was known in the art that such pedestals in integrated circuits my have a finish applied to them, as disclosed by Carter. One would have been motivated to have a gold or silver finish applied to the pedestals since gold and silver promote the bonding of the wires to the pedestals and are highly conductive.

Response to Arguments

14. Applicant's arguments with respect to claims 16 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is

(571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
February 18, 2009